directed to a timing recovery system for generating a set of sampling clock signals for use by respective subsystems of an overall system. The sampling clock signals are associated with a set of transmitted input signals. The system includes a set of phase detectors that generate phase errors for the corresponding sampling clock signals, a set of loop filters coupled to the corresponding phase detectors to generate filtered phase errors, a set of digital-to-analog (D/A) converters coupled to the loop filters to generate analog filtered phase errors, and a set of oscillators coupled to the corresponding D/A converters to generate the sampling clock signals. The sampling clock signals are then transmitted to the respective subsystems and used to independently clock those subsystems. Significantly, the claimed invention relates to a system for generating sampling clock signals for several input signals that have been transmitted over a medium and that, consequently, may have been subjected to different transmission medium characteristics. One example of a medium characteristic is the response of a transmission cable. This aspect of the claimed invention is not taught or suggested by the references of record.

The Brede et al. patent discloses a phase locked loop (PLL) that, in one embodiment, includes two PLLs. As is shown in FIGS. 3 and 4, the outputs from the respective PLLs 100a and 100b are introduced to a phase comparator 460, which outputs an analog output that is proportional to the phase difference between the two signals.

Thus, the output of the circuit in the Brede et al. patent is a single signal, and is not a sampling clock signal. Thus, pending claim 41, which produces plural sampling clock signals, and then delivers those signals to respective subsystems, is not anticipated by the Brede et al. patent.

Moreover, Alder et al. does not suggest or teach a system that provides sampling clock signals for a set of input signals. As shown in Figure 1, Alder et al. discloses a system that generates two signals (V0 and V02) from a single input signal (Vref). Hence, Brede at al. and Alder et al. considered either separately or in combination do not teach or suggest the claimed combination.

Accordingly, applicant respectfully submits that independent claim 41, the associated independent method claim 58 and all claims that depend on those claims are allowable over the cited art.

CONCLUSION

It is respectfully submitted that all of the pending claims are in condition for allowance, and an early notice of allowance is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____
Stephen D. Burbach
Reg. No. 40,285
626/795-9900

SDB/cbc

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Specification:

Please amend the two paragraphs under CROSS-REFERENCE TO RELATED APPLICATIONS on page 2 as follows:

The present application is a continuation of U.S. Patent application Serial No. 09/437,721, filed November 9, 1999 which claims priority of the following provisional applications, the contents of each of which are herein incorporated by reference: Serial Number 60/107,874 entitled "Apparatus for, and Method of, Distributing Clock Signals in a Communications System" filed on November 9, 1998; Serial Number 60/108,319 entitled "Gigabit Ethernet Transceiver" filed on November 13, 1998; Serial Number 60/108,648 entitled "Clock Generation and Distribution in an Ethernet Transceiver" filed on November 16, 1998 and Serial Number 60/130,616 entitled "Multi-Pair Gigabit Ethernet Transceiver" filed on April 22, 1999.

The present invention is related to the following co-pending applications filed on the same day as the present invention and assigned to the same assignee, the contents of each of which are herein incorporated by reference: Serial Number [____] 09/437,724 entitled "Switching Noise Reduction in a Multi-Clock Domain Transceiver" and Serial Number [____] 09/437,719 entitled "Multi-Pair Gigabit Ethernet Transceiver".

Please insert the following paragraph on page 6, after line 17 and before line 18, as follows:

FIG 5A shows another embodiment for generating the sampling clock signals.

Please amend the second full paragraph on page 15 as follows:

The 4-D output of the trellis decoder 38 is provided to the PCS receive section 204R. The receive section 204R of the PCS block de-scrambles and decodes the symbol stream, then passes the decoded packets and idle stream to the receive section [202T] 202R of the GMII block which passes them to the MAC module. The 4-D outputs, which are the error and tentative decision, respectively, are provided to the timing recovery block 222, whose output controls the sampling time of the A/D converter 216. One of the four components of the error and one of the four components of the tentative decision correspond to the receiver shown in FIG. 2, and are provided to the adaptive gain stage 34 of the FFE 26 to adjust the gain of the equalizer signal path. The error component portion of the decoder output signal is also provided, as a control signal, to adaptation circuitry incorporated in each of the adaptive filters 230 and 232. Adaptation circuitry is used for the updating and training process of filter coefficients.

Please amend the paragraph beginning at line 23 on page 24 as follows:

It is important to note that, referring to FIG. 5, the function performed by the combination of an NCO (508, 518, 528, 538) followed by a phase selector (610, 620, 630, 640, 650, 660) can be implemented by analog circuitry. The analog circuitry can be described as follows. Each of the filtered phase errors outputted from the loop filters (506, 516, 526, 536) would be inputted to a D/A converter to be converted to analog form. Each of the analog filtered phase errors would then be inputted to a voltage-controlled oscillator (VCO). The VCOs would produce the clock signals. The VCOs can be implemented with well-known analog techniques such as those using varactor diodes. <u>This embodiment is shown in FIG. 5A.</u>

<u>In The Claims</u>:

Please amend claim 41, and add new claims 43 - 60 as follows:

41. (Amended) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system comprising:

(a) a set of phase detectors generating phase errors for the corresponding sampling clock signals;

(b) a set of loop filters coupled to the corresponding phase detectors, the loop filters receiving the corresponding phase errors and generating filtered phase errors;

(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the corresponding D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals, wherein the sampling clock signals so generated are transmitted to respective subsystems.

42. (Unchanged)The timing recovery system of claim 41 wherein the oscillators comprise varactor diodes.

43. (New) The timing recovery system of claim 41 wherein the set of clock signals further comprises a receive clock signal and wherein each of the processing subsystems further comprises a digital section, the digital sections operating in accordance with the receive clock signal.

44. (New) The timing recovery system of claim 43 wherein the receive clock signal is related to one of the sampling clock signals.

45. (New) The timing recovery system of claim 44 further comprising a first adder and a receive clock phase selector, the first adder receiving one of the phase control signals and a receive clock offset and generating a phase shift value, the receive clock phase selector receiving the phase shift value and generating the receive clock signal.

46. (New) The timing recovery system of claim 45 wherein the phase shift value comprises a set of phase steps and wherein the receive clock phase selector receives the phase shift value in the form of consecutive phase steps.

47. (New) The timing recovery system of claim 41 wherein the set of clock signals further comprises a transmit clock signal and wherein each of the subsystems further comprises a transmit section, the transmit sections operating in accordance with the transmit clock signal.

48. (New) The timing recovery system of claim 47 further comprising a transmit clock phase selector, the transmit clock phase selector receiving a transmit clock offset and generating the transmit clock signal.

49. (New) The timing recovery system of claim 48 wherein the transmit clock offset is equal to zero.

50. (New) The timing recovery system of claim 47 wherein the transmit clock signal is related to one of the sampling clock signals.

51. (New) The timing recovery system of claim 50 further comprising a transmit clock phase selector, the transmit clock phase selector receiving one of the phase control signals and generating the transmit clock signal.

52. (New) The timing recovery system of claim 41 wherein each of the phase detectors receives a corresponding slicer error and a corresponding tentative decision from a decoding system.

53. (New) The timing recovery system of claim 52 wherein each of the phase detectors comprises a lattice structure, the lattice structure comprising two delay elements, two multipliers and an adder, the lattice structure generating a pre-cursor phase error by multiplying the corresponding tentative decision by a delayed version of the corresponding slicer error and generating a post-cursor phase error by multiplying the corresponding slicer error by a delayed version of the corresponding tentative decision and combining the pre-cursor and post-cursor phase errors to produce the corresponding phase error.

54. (New) The timing recovery system of claim 53 wherein at least one of the phase detectors further receives an offset input from a control unit and wherein the associated lattice structure combines the pre-cursor, post-cursor phase errors and the offset input to produce the corresponding phase error.

55. (New) The timing recovery system of claim 41 wherein at least one of the loop filters comprises a first filter for accumulating a number of consecutive values of one of the phase errors to produce a filtered phase error.

56. (New) The timing recovery system of claim 41 wherein at least one of the loop filters comprises a first filter for accumulating a number of consecutive values of one of the phase errors to produce a sum value, a second filter for integrating the sum value to produce an integral value and an adder for combining the sum value and the integral value to produce a filtered phase error.

57. (New) The timing recovery system of claim 56 wherein the second filter includes a multiplier for scaling the integrated sum value by a scale factor to produce the integral value.

58. (New) A method for generating a set of clock signals in a system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding set of input signals, the system comprising a set of subsystems, each of the subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the method comprising the operations of:

(a) generating a phase error for each of the sampling clock signals from a corresponding phase detector using signals associated with a corresponding plurality of input signals;

(b) inputting each of the phase errors to a corresponding loop filter;

(c) generating filtered phase errors from the corresponding loop filters;

(d) converting the filtered phase errors to analog filtered phase errors;

(e) inputting each of the analog filtered phase errors to a corresponding oscillator;

and

(f) generating sampling clock signals from the corresponding oscillators.

59. (New) A method for generating a set of clock signals in a system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals and a receive clock signal, the system comprising a set of subsystems, each of the subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, each of the subsystems comprising a digital section, each of the digital sections operating in accordance with the receive clock signal, the method comprising the operations of:

(a) receiving a plurality of transmitted signals;

(b) generating phase control signals associated with each of the plurality of transmitted signals;

(c) generating a receive phase control signal for the receive clock signal in accordance with at least one of the phase control signals;

(d) generating the sampling clock signals in accordance with the corresponding phase control signals;

and

(e) generating the receive clock signal in accordance with the receive phase control signal.

60. (New) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals and a receive clock signal, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, each of the processing subsystems comprising a digital section, each of the digital sections operating in accordance with the receive clock signal, the timing recovery system comprising:

(a) a decoder for generating a plurality of signals associated with the plurality of transmitted signals;

and

(b) a timing recovery circuit for receiving the signals generated by the decoder, and for generating phase control signals associated with each of the plurality of transmitted signals and a receive phase control signal for the receive clock signal in accordance with at least one of the phase control signals, wherein the timing recovery circuit generates the sampling clock signals in accordance with the corresponding phase control signals and generates the receive clock signal in accordance with the receive phase control signal.